

T66H0002A

160 output LCD Segment/Common Driver IC

FEATURES

- Number of LCD drive outputs : 160
- Supply voltage for LCD drive :
+15.0 to +45.0 V
- Supply voltage for the logic system :
+2.5 to +5.5 V
- Low power consumption
- Low output impedance

DESCRIPTION

The T66H0002A is a 160-output segment/common driver IC suitable for driving large/medium scale dot matrix LCD panels, and is used in personal computers/work stations. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LCD module. The T66H002A is good both as a segment driver and a common driver, and it can create a low power consuming, high resolution LCD.

Segment mode:

1. Shift clock frequency : 14 MHz (MAX.) (VDD=+5.0V±10%)
: 8 MHz(MAX.) (VDD=+2.5V~+4.5V)
2. Adopts a data bus system
3. 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
4. Automatic transfer function of an enable signal
5. Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 160 bits of input data
6. Line latch circuits are reset when / DISPOFF low active

Common mode:

- Shift clock frequency : 4 MHz (MAX.)
- Built-in 160-bit bi-directional shift register (divisible into 80 bits x 2)
- Available in a single mode (160-bit shift register) or in a dual mode (80-bit shift register x 2)
 - a. Y1 → Y160 Single mode
 - b. Y160 → Y1 Single mode
 - c. Y1 → Y80, Y81 → Y160 Dual mode
 - d. Y160 → Y81, Y80 → Y1 Dual mode

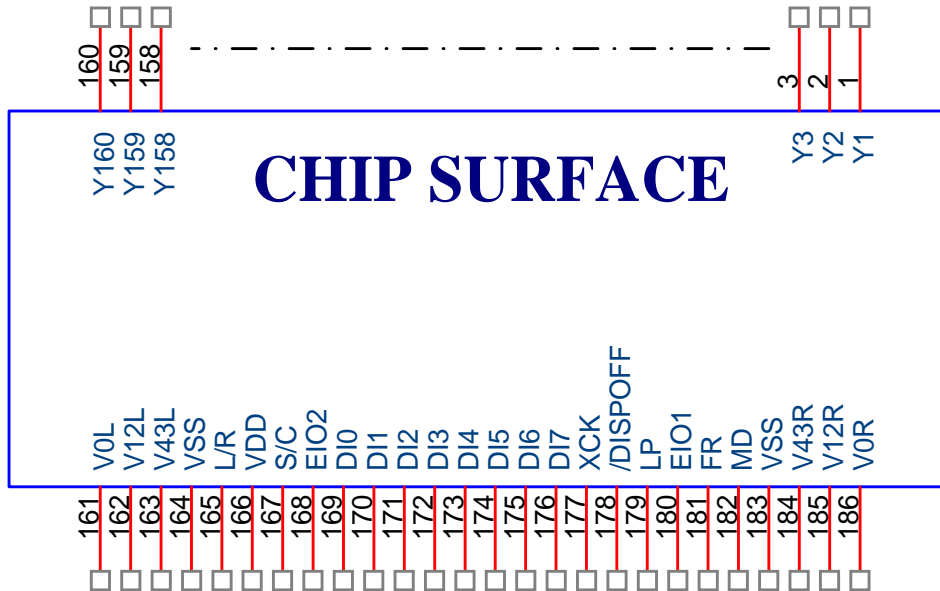
The above 4 shift directions are pin selectable

Part Number Examples

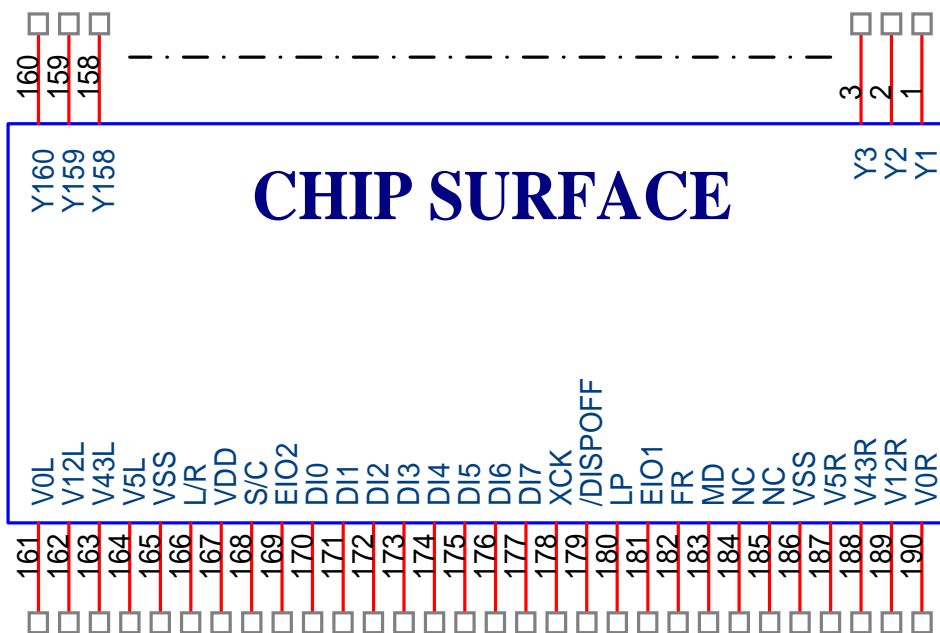
| Part No. | Pkg. | Description |
|--------------|------|---------------------------------|
| T66H0002A-Y | TCP | Pitch 0.18mm, refer to Appendix |
| T66H0002A-AY | TCP | Pitch 0.22mm, refer to Appendix |
| T66H0002A | COG | Refer to Pads List |

PIN CONNECTIONS

186-PIN TCP



190-PIN TCP



PIN DESCRIPTION

For 186-PIN TCP

| PIN NO. | SYMBOL | I/O | DESCRIPTION |
|------------|-------------------------------------|-----|---|
| 1 to 160 | Y1-Y160 | O | LCD drive output |
| 161, 186 | V _{0L} , V _{0R} | - | Power supply for LCD drive |
| 162, 185 | V _{12L} , V _{12R} | - | Power supply for LCD drive |
| 163, 184 | V _{43L} , V _{43R} | - | Power supply for LCD drive |
| 166 | VDD | - | Power supply for logic system (+2.5V to +5.5V) |
| 167 | S/C | I | Segment mode/common mode selection |
| 168, 180 | EIO ₂ , EIO ₁ | I/O | Input/output for chip select or data od shift register |
| 169 to 175 | DI ₀ -DI ₆ | I | Display data input at segment mode |
| 176 | DI ₇ | I | Display data input at segment mode/Dual mode data input |
| 177 | XCK | I | Clock input for taking display data at segment mode |
| 178 | /DISPOFF | I | Control input for output of non-select level |
| 179 | LP | I | Latch pules input /shift clock input for shift register |
| 181 | FR | I | AC-converting signal input for LCD drive waveform |
| 165 | L/R | I | Display data shift direction selection |
| 182 | MD | I | Mode selection input |
| 164,183 | VSS | - | Ground(0V) |

For 190-PIN TCP

| PIN NO. | SYMBOL | I/O | DESCRIPTION |
|------------|-------------------------------------|-----|---|
| 1 to 160 | Y1-Y160 | O | LCD drive output |
| 161, 190 | V _{0L} , V _{0R} | - | Power supply for LCD drive |
| 162, 189 | V _{12L} , V _{12R} | - | Power supply for LCD drive |
| 163, 188 | V _{43L} , V _{43R} | - | Power supply for LCD drive |
| 164,187 | V _{5L} , V _{5R} | - | Power supply for LCD drive |
| 167 | VDD | - | Power supply for logic system (+2.5V to +5.5V) |
| 168 | S/C | I | Segment mode/common mode selection |
| 169, 181 | EIO ₂ , EIO ₁ | I/O | Input/output for chip select or data od shift register |
| 170 to 176 | DI ₀ -DI ₆ | I | Display data input at segment mode |
| 177 | DI ₇ | I | Display data input at segment mode/Dual mode data input |
| 178 | XCK | I | Clock input for taking display data at segment mode |
| 179 | /DISPOFF | I | Control input for output of non-select level |
| 180 | LP | I | Latch pules input /shift clock input for shift register |
| 182 | FR | I | AC-converting signal input for LCD drive waveform |
| 166 | L/R | I | Display data shift direction selection |
| 183 | MD | I | Mode selection input |
| 184,185 | NC | I | Not Connection |
| 165,185 | VSS | - | Ground(0V) |

INPUT/OUTPUT CIRCUITS

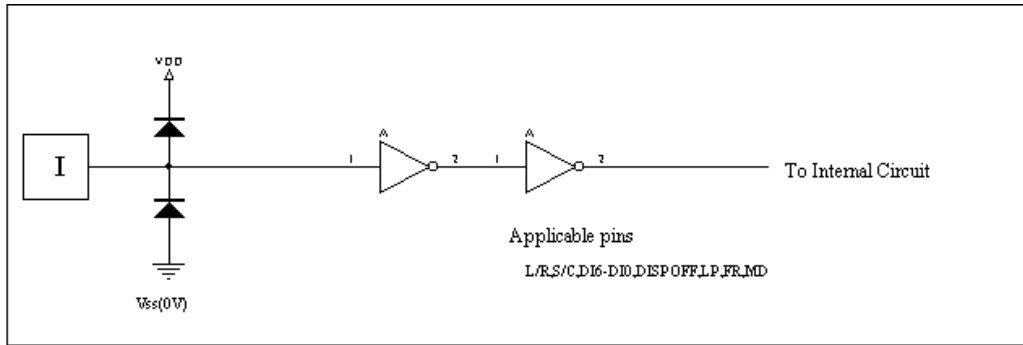


Fig1. Input Circuit (1)

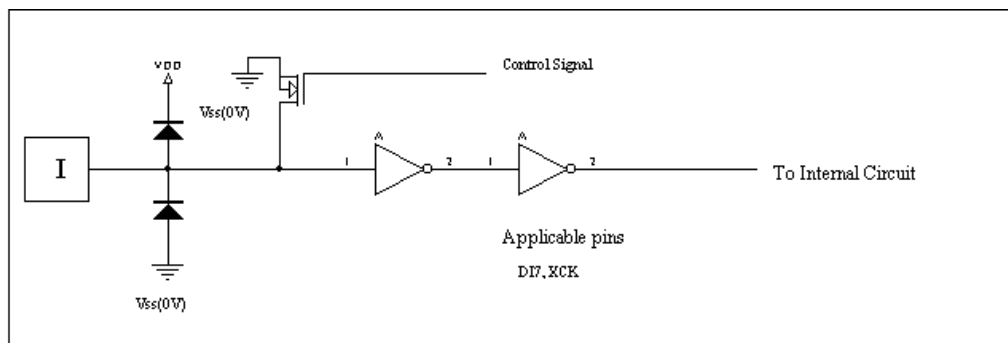


Fig2. Input Circuit (2)

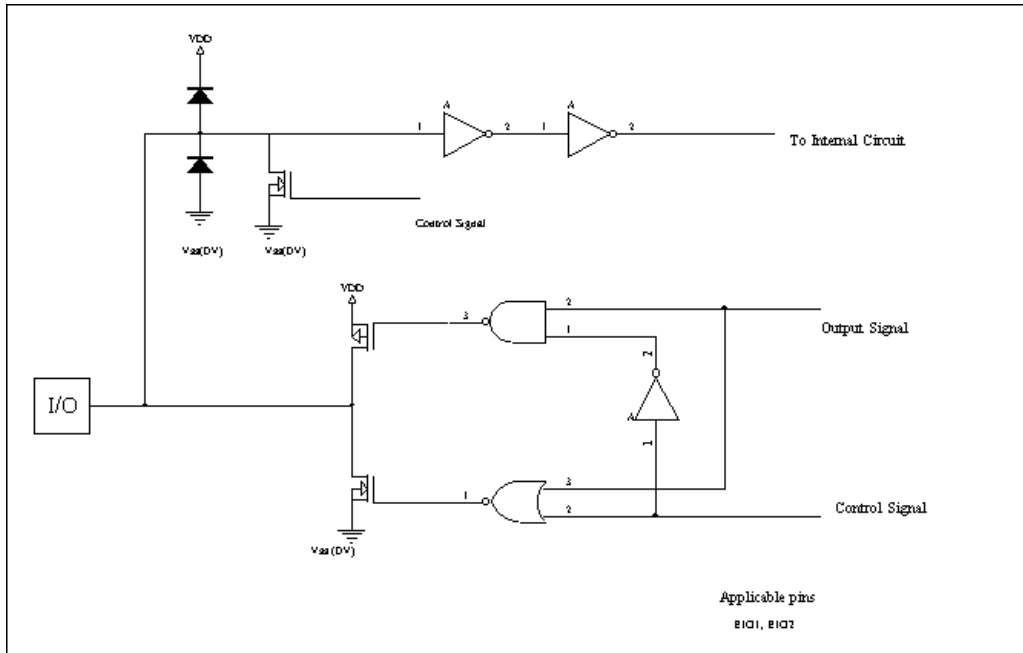


Fig4. Input/Output Circuit

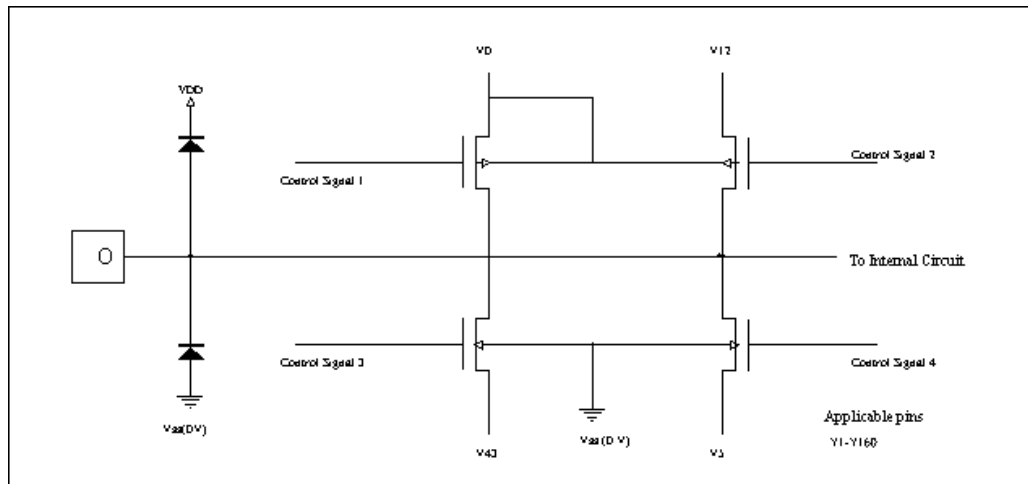
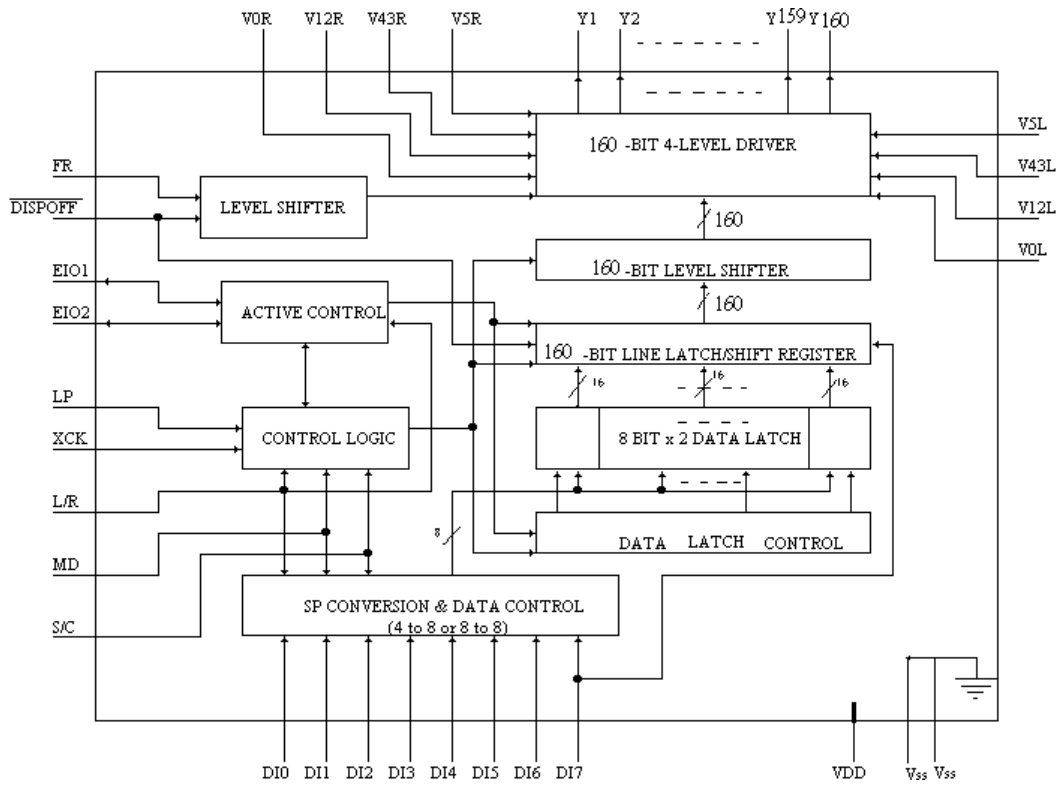


Fig 5 LCD Drive Output Circuit

BLOCK DIAGRAM



FUNCTIONAL OPERATIONS OF EACH BLOCK

| BLOCK | FUNCTION |
|------------------------------|--|
| Active Control | In case of segment mode, controls the selection or non-selection of the chip. Following and LP signal input, and after the chip selection signal is input, a selection signal is generated internally until 160 bits of data have been read in. Once data input has been completed, a selection signal for cascade connection is output, and the chip is non-selected. In case of common mode, controls the input/output data of bi-directional pins. |
| SP Conversion & Data Control | In case of segment mode, keeps input data which are 2 clocks of XCK at 4-bit parallel input mode in latch circuit, or keeps input data which are 1 clock of XCK at 8-bit parallel input mode in latch circuit; after that they are put on the internal data 8 bits at a time. |
| Data Latch Control | In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic. For every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit. |
| Data Latch | In case of segment mode, latches the data on the data bus. The latch state of each LCD drive output pin is controlled by the control logic and the data latch control; 160 bits of data are read in 20 sets of 8 bits. |
| Line Latch/Shift Register | In case of segment mode, all 160 bits which have been read into the data latch are simultaneously latched at the falling edge of the LP signal, and are output to the level shifter block. In case of common mode, shifts data from the data input pin at the falling edge of the LP signal. |
| Level Shifter | The logic voltage signal is level-shifted to the LCD drive voltage level, and in output to the driver block. |
| 4-Level driver | Drives the LCD drive output pins from the line latch/shift register data, and selects one of 4 levels($V_0, V_{12}, V_{43},$ or V_{ss}) based on the S/C, FR and /DISPOFF signals. |
| Control Logic | Controls the operation of each block. In case of segment mode, when an LP signal has been input, all blocks are rest and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission is controlled, 160 bits of data are read in , and the chip in non-selected. In case of common mode, controls the direction of data shift. |

FUNCTIONAL DESCRIPTION

Pin Functions

(Segment mode)

| SYMBOL | FUNCTION |
|---|--|
| V _{DD} | Logic system power supply pin, connected to +2.5 to +5.5 V. |
| V _{SS} | Ground pin, connected to 0 V. |
| V _{0L} , V _{0R} V _{12L} , V _{12R} V _{43L} , V _{43R} | <p>Bias power supply pins for LCD drive voltage</p> <ul style="list-style-type: none"> • Normally use the bias voltages set by a resistor divider. • Ensure that voltages are set such that V_{SS} < V₄₃ < V₁₂ < V₀. • V_{iL} and V_{iR} (i = 0, 12, 43) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin. |
| DI ₇ , DI ₀ | <p>Input pins for display data</p> <ul style="list-style-type: none"> • In 4-bit parallel input mode, input data into the 4 pins, DI₃-DI₀. Connect DI₇-DI₄ to V_{SS} or V_{DD}. • In 8-bit parallel input mode, input data into the 8 pins, DI₇-DI₀. • Refer to “RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS” in Functional Operations. |
| XCK | <p>Clock input pin for taking display data</p> <ul style="list-style-type: none"> • Data is read at the falling edge of the clock pulse. |
| LP | <p>Latch pulse input pin for display data</p> <ul style="list-style-type: none"> • Data is latched at the falling edge of the clock pulse. |
| L/R | <p>Input pin for selecting the reading direction of display data</p> <ul style="list-style-type: none"> • When set to V_{SS} level “L”, data is read sequentially from Y₁₆₀ to Y₁. • When set to V_{DD} level “H”, data is read sequentially from Y₁ to Y₁₆₀. • Refer to “RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS” in Functional Operations. |
| /DISPOFF | <p>Control input pin for output of non-select level</p> <ul style="list-style-type: none"> • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level “L”, the LCD drive output pins (Y₁-Y₁₆₀) are set to level V_{SS}. • When set to “L”, the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of /DISPOFF. When the /DISPOFF function is canceled, the driver outputs non-select level (V₁₂ or V₄₃), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, it can not output the reading data correctly. • Table of truth values is shown in “TRUTH TABLE” in Functional Operations. |
| FR | <p>AC signal input pin for LCD drive waveform</p> <ul style="list-style-type: none"> • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins’ output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth values is shown in “TRUTH TABLE” in Functional Operations. |

| SYMBOL | FUNCTION |
|-------------------------------------|---|
| MD | Mode selection pin <ul style="list-style-type: none"> • When set to V_{SS} level “L”, 4 bit parallel input mode is set. • When set to V_{DD} level “H”, 8 bit parallel input mode is set. • Refer to “RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS” in Functional Operations. |
| S/C | Segment mode/common mode selection pin <ul style="list-style-type: none"> • When set to V_{DD} level “H”, segment mode is set. |
| EIO ₁ , EIO ₂ | Input/output pins for chip selection <ul style="list-style-type: none"> • When L/R input is at V_{SS} level “L”, EIO₁ is set for output , and EIO₂ is set for input. • When L/R input is at V_{DD} level “H”, EIO₁ is set for input , and EIO₂ is set for output. • During output , set to “H” while LP/XCK is “H” and after 160 bits of data have been read , set to “L” for one cycle (from falling edge to falling edge of XCK), after which it returns to “H”. • During input , the chip is selected while EI is set to “L” after the LP signal is input. The chip is non-selected after 160 bits of data have been read. |
| Y ₁ -Y ₁₆₀ | LCD drive output pins <ul style="list-style-type: none"> • Corresponding directly to each bit of the data latch, one level (V₀, V₁₂, V₄₃ or V_{SS}) is selected and output. • Table of truth values is shown in “TRUTH TABLE” in Functional Operations. |

(Common mode)

| SYMBOL | FUNCTION |
|---|--|
| V _{DD} | Logic system power supply pin, connected to +2.5 to +5.5 V. |
| V _{SS} | Ground pin, connected to 0 V. |
| V _{0L} , V _{0R} V _{12L} , V _{12R} V _{43L} , V _{43R} | Bias power supply pins for LCD drive voltage <ul style="list-style-type: none"> • Normally use the bias voltages set by a resistor divider. • Ensure that voltages are set such that V_{SS} < V₄₃ < V₁₂ < V₀. • V_{iL} and V_{iR} (i = 0 , 12 , 43) must connect to an external power supply , and supply regular voltage which is assigned by specification for each power pin. |
| EIO ₁ | Shift data input/output pin for bi-directional shift register <ul style="list-style-type: none"> • Output pin when L/R is at V_{SS} level “L” , input pin when L/R is at V_{DD} level “H”. • When L/R = H, EIO₁ is used as input pin, it will be pulled down. • When L/R = L, EIO₁ is used as output pin, it won’t be pulled down. • Refer to “ RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS” in Functional Operations. |
| EIO ₂ | Shift data input/output pin for bi-directional shift register <ul style="list-style-type: none"> • Input pin when L/R is at V_{SS} level “L” , output pin when L/R is at V_{DD} level “H”. • When L/R = L, EIO₂ is used as input pin, it will be pulled down. • When L/R = H, EIO₂ is used as output pin, it won’t be pulled down. • Refer to “ RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS” in Functional Operations. |
| LP | Shift Clock pulse input pin for bi-directional shift register <ul style="list-style-type: none"> • Data is shifted at the falling edge of the clock pulse. |
| L/R | Input pin for selecting the shift direction of bi-directional shift register <ul style="list-style-type: none"> • Data is shifted from Y₁₆₀ to Y₁ when set to V_{SS} level “L” , and data is shifted from Y₁ to Y₁₆₀ when set to V_{DD} level “H”. • Refer to “ RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS” in Functional Operations. |
| /DISPOFF | Control input pin for output of non-select level <ul style="list-style-type: none"> • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level “L”, the LCD drive output pins (Y₁-Y₁₆₀) are set to level V₅. • When set to “L”, the contents of the shift register are reset to not reading data. When the /DISPOFF function is canceled , the driver outputs non-select level (V₁₂ or V₄₃), and the shift data is read at the next falling edge of the LP. At that time , if /DISPOFF removal time does not correspond to what is shown in AC characteristic, the shift data is not read correctly. • Table of truth value is shown in “TRUTH TABLE” in Functional Operations. |
| FR | AC signal input pin for LCD drive waveform <ul style="list-style-type: none"> • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins’ output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth value is shown in “TRUTH TABLE” in Functional Operations. |

| SYMBOL | FUNCTION |
|----------------------------------|--|
| MD | Mode selection pin • When set to V _{SS} level “L”, single operation is selected ; when set to V _{DD} level “H”, dual mode operation is selected. • Refer to “ RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS ” in Functional Operations. |
| DI ₇ | Dual mode data input pin • According to the data shift direction of the data shift register , data can be input starting from the 81 st bit. • When the chip is used in dual mode , DI ₇ will be pulled down. • When the chip is used in single mode , DI ₇ won't be pulled down. • Refer to “ RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS ” in Functional Operations. |
| S/C | Segment mode/common mode selection pin • When set to V _{SS} level “L, common mode is set. |
| DI ₆ -DI ₀ | Not used • Connect DI ₆ -DI ₀ to V _{SS} or V _{DD} , avoiding floating. |
| XCK | Not used • XCK is pulled down in common mode, so connect to V _{SS} or open. |
| Y ₁ -Y ₁₆₀ | LCD drive output pins • Corresponding directly to each bit of the data latch, one level (V ₀ , V ₁₂ , V ₄₃ or V _{SS}) is selected and output. • Table of truth values is shown in “ TRUTH TABLE ” in Functional Operations. |

Functional Operations

TRUTH TABLE

(Segment Mode)

| FR | Latch Data | /DISPOFF | LCD Drive Output Voltage Level (Y ₁ -Y ₁₆₀) |
|----|------------|----------|--|
| L | L | H | V ₄₃ |
| L | H | H | V _{SS} |
| H | L | H | V ₁₂ |
| H | H | H | V ₀ |
| X | X | L | V _{SS} |

(Common Mode)

| FR | Latch Data | /DISPOFF | LCD Drive Output Voltage Level (Y ₁ -Y ₁₆₀) |
|----|------------|----------|--|
| L | L | H | V ₄₃ |
| L | H | H | V ₀ |
| H | L | H | V ₁₂ |
| H | H | H | V _{SS} |
| X | X | L | V _{SS} |

NOTES:

- V_{SS} < V₄₃ < V₁₂ < V₀, L: V_{SS} (0 V), H: V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.

Supply regular voltage which is assigned by specification for each power pin.

RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS

(Segment Mode)

(a) 4-bit Parallel Input Mode

| MD | L/R | EIO ₁ | EIO ₂ | DATA INPUT | NUMBER OF CLOCKS | | | | | | |
|----|-----|------------------|------------------|-----------------|------------------|------------------|------------------|-----|------------------|------------------|------------------|
| | | | | | 40 Clock | 39 Clock | 38 Clock | ... | 3 Clock | 2 Clock | 1 Clock |
| L | L | Output | Input | DI ₀ | Y ₁ | Y ₅ | Y ₉ | ... | Y ₁₄₉ | Y ₁₅₃ | Y ₁₅₇ |
| | | | | DI ₁ | Y ₂ | Y ₆ | Y ₁₀ | ... | Y ₁₅₀ | Y ₁₅₄ | Y ₁₅₈ |
| | | | | DI ₂ | Y ₃ | Y ₇ | Y ₁₁ | ... | Y ₁₅₁ | Y ₁₅₅ | Y ₁₅₉ |
| | | | | DI ₃ | Y ₄ | Y ₈ | Y ₁₂ | ... | Y ₁₅₂ | Y ₁₅₆ | Y ₁₆₀ |
| L | H | Input | Output | DI ₀ | Y ₁₆₀ | Y ₁₅₆ | Y ₁₅₂ | ... | Y ₁₂ | Y ₈ | Y ₄ |
| | | | | DI ₁ | Y ₁₅₉ | Y ₁₅₅ | Y ₁₅₁ | ... | Y ₁₁ | Y ₇ | Y ₃ |
| | | | | DI ₂ | Y ₁₅₈ | Y ₁₅₄ | Y ₁₅₀ | ... | Y ₁₀ | Y ₆ | Y ₂ |
| | | | | DI ₃ | Y ₁₅₇ | Y ₁₅₃ | Y ₁₄₉ | ... | Y ₉ | Y ₅ | Y ₁ |

(b) 8 bit Parallel input Mode

| MD | L/R | EIO ₁ | EIO ₂ | DATA INPUT | NUMBER OF CLOCKS | | | | | | |
|----|-----|------------------|------------------|-----------------|------------------|------------------|------------------|-----|------------------|------------------|------------------|
| | | | | | 20 Clock | 19 Clock | 18 Clock | ... | 3 Clock | 2 Clock | 1 Clock |
| H | L | Output | Input | DI ₀ | Y ₁ | Y ₉ | Y ₁₇ | ... | Y ₁₃₇ | Y ₁₄₅ | Y ₁₅₃ |
| | | | | DI ₁ | Y ₂ | Y ₁₀ | Y ₁₈ | ... | Y ₁₃₈ | Y ₁₄₆ | Y ₁₅₄ |
| | | | | DI ₂ | Y ₃ | Y ₁₁ | Y ₁₉ | ... | Y ₁₃₉ | Y ₁₄₇ | Y ₁₅₅ |
| | | | | DI ₃ | Y ₄ | Y ₁₂ | Y ₂₀ | ... | Y ₁₄₀ | Y ₁₄₈ | Y ₁₅₆ |
| | | | | DI ₄ | Y ₅ | Y ₁₃ | Y ₂₁ | ... | Y ₁₄₁ | Y ₁₄₉ | Y ₁₅₇ |
| | | | | DI ₅ | Y ₆ | Y ₁₄ | Y ₂₂ | ... | Y ₁₄₂ | Y ₁₅₀ | Y ₁₅₈ |
| | | | | DI ₆ | Y ₇ | Y ₁₅ | Y ₂₃ | ... | Y ₁₄₃ | Y ₁₅₁ | Y ₁₅₉ |
| | | | | DI ₇ | Y ₈ | Y ₁₆ | Y ₂₄ | ... | Y ₁₄₄ | Y ₁₅₂ | Y ₁₆₀ |
| H | H | Input | Output | DI ₀ | Y ₁₆₀ | Y ₁₅₂ | Y ₁₄₄ | ... | Y ₂₄ | Y ₁₆ | Y ₈ |
| | | | | DI ₁ | Y ₁₅₉ | Y ₁₅₁ | Y ₁₄₃ | ... | Y ₂₃ | Y ₁₅ | Y ₇ |
| | | | | DI ₂ | Y ₁₅₈ | Y ₁₅₀ | Y ₁₄₂ | ... | Y ₂₂ | Y ₁₄ | Y ₆ |
| | | | | DI ₃ | Y ₁₅₇ | Y ₁₄₉ | Y ₁₄₁ | ... | Y ₂₁ | Y ₁₃ | Y ₅ |
| | | | | DI ₄ | Y ₁₅₆ | Y ₁₄₈ | Y ₁₄₀ | ... | Y ₂₀ | Y ₁₂ | Y ₄ |
| | | | | DI ₅ | Y ₁₅₅ | Y ₁₄₇ | Y ₁₃₉ | ... | Y ₁₉ | Y ₁₁ | Y ₃ |
| | | | | DI ₆ | Y ₁₅₄ | Y ₁₄₆ | Y ₁₃₈ | ... | Y ₁₈ | Y ₁₀ | Y ₂ |
| | | | | DI ₇ | Y ₁₅₃ | Y ₁₄₅ | Y ₁₃₇ | ... | Y ₁₇ | Y ₉ | Y ₁ |

(Common Mode)

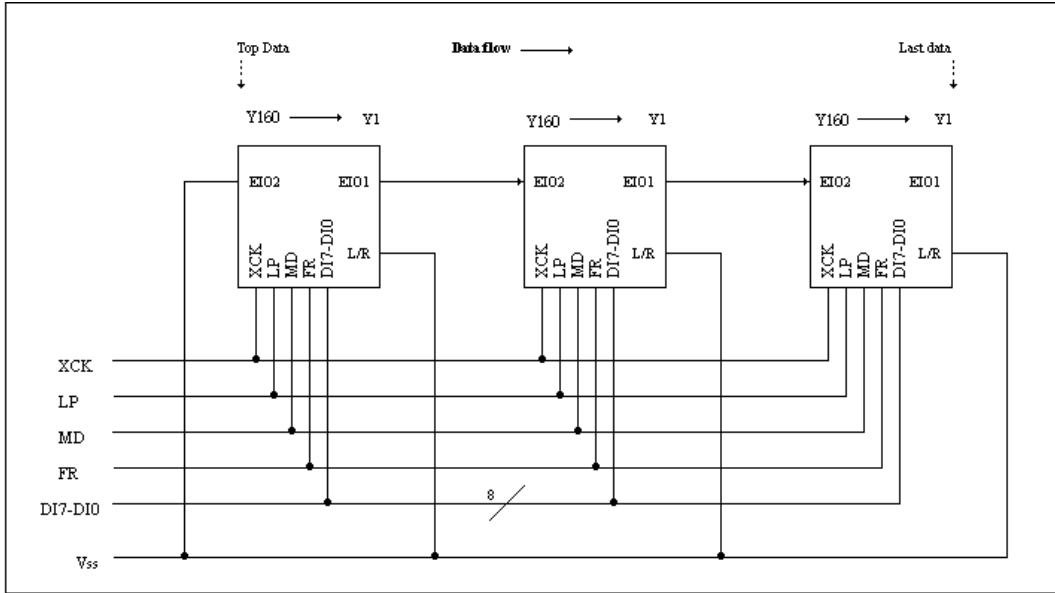
| MD | L/R | Data Transfer Direction | EIO ₁ | EIO ₂ | DI ₇ |
|---------------|-----|--|------------------|------------------|-----------------|
| L (Single) | L | Y ₁₆₀ → Y ₁ | Output | Input | X |
| | H | Y ₁ → Y ₁₆₀ | Input | Output | X |
| H (Dual) | L | Y ₁₆₀ → Y ₈₁ Y ₈₀ → Y ₁ | Output | Input | Input |
| | H | Y ₁ → Y ₈₀ Y ₈₁ → Y ₁₆₀ | Input | Output | Input |

NOTES:

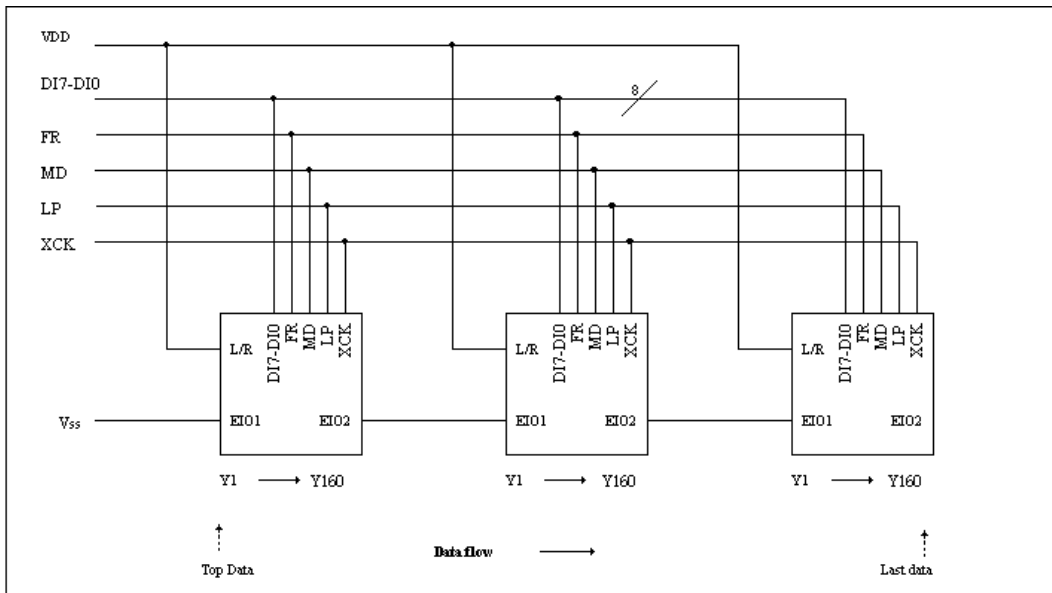
- L: V_{SS} (0 V), H: V_{DD} (+2.5 to +5.5 V), X: Don't care
- “Don't care” should be fixed to “H” or “L”, avoiding floating.

CONNECTION EXAMPLES OF PLURAL SEGMENT DRIVERS

(a) When L/R = "L"

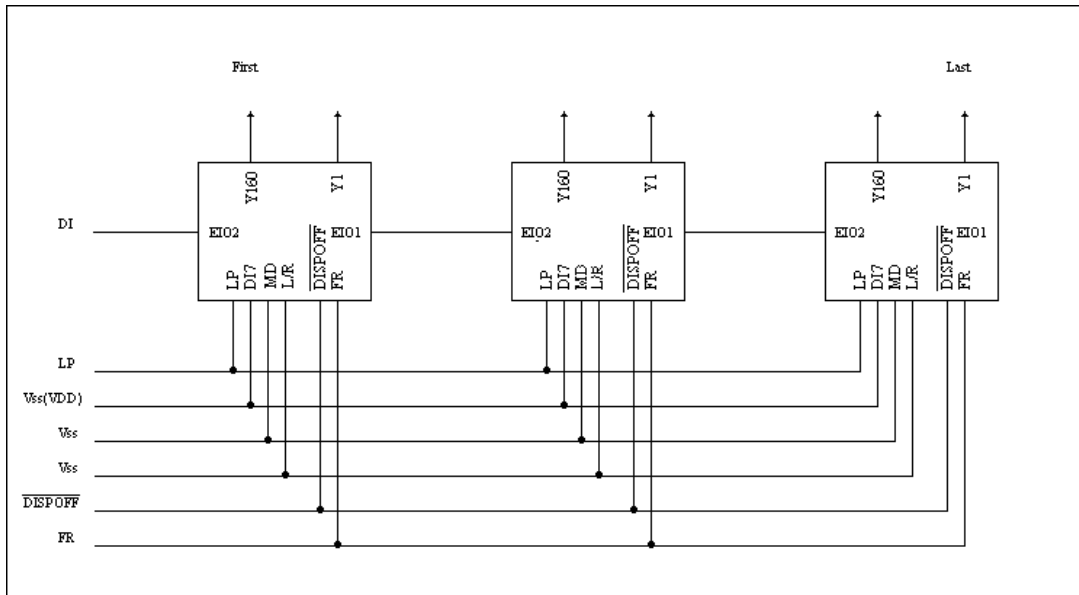


(b) When L/R = "H"

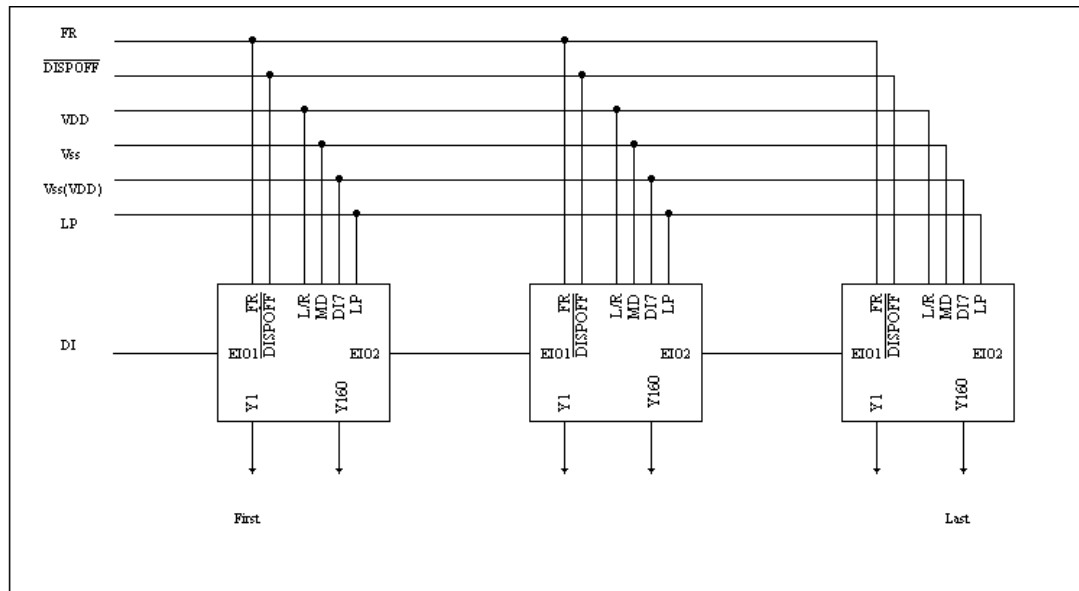


CONNECTION EXAMPLES FOR PLURAL COMMON DRIVERS

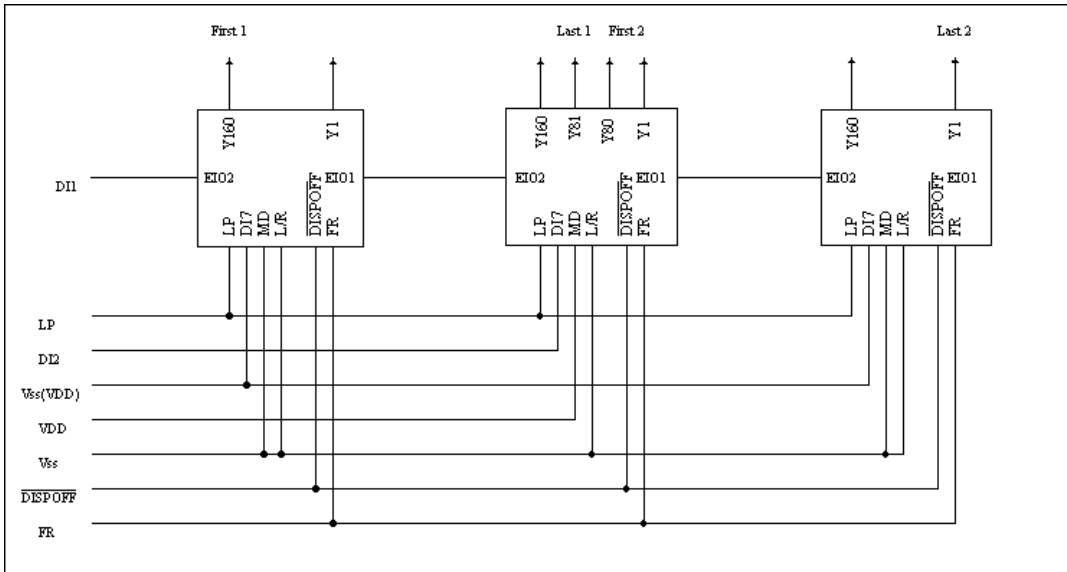
(a) Single Mode (L/R = "L")



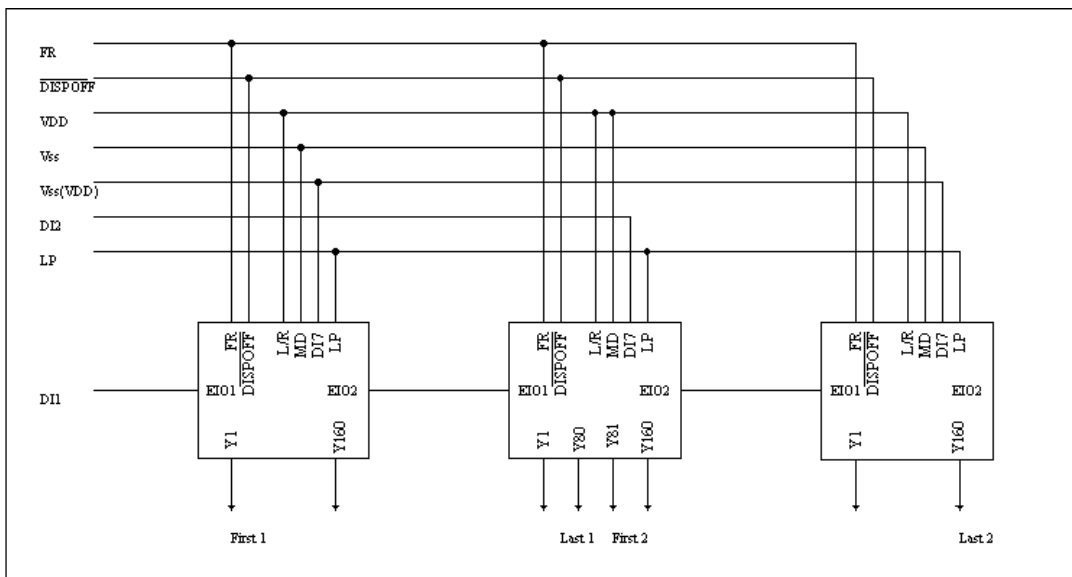
(b) Single Mode (L/R = "H")



(c) Dual Mode (L/R = "L")



(d) Dual Mode (L/R = "H")



PRECAUTIONS

Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The details are as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.
- It is advisable to connect the serial resistor (50 to 100 Ω) or fuse to the LCD drive power V_0 of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on /DISPOFF function. After that, cancel the /DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level V_s on /DISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power. When connecting the power supply, follow the recommended sequence shown here.



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | APPLICABLE PINS | RATING | UNIT | NOTE |
|---------------------|------------------|--|-------------------------------|------|------|
| Supply voltage(1) | V _{DD} | V _{DD} | -0.3 to +7.0 | V | 1,2 |
| Supply voltage(2) | V ₀ | V _{0L} , V _{0R} | -0.3 to +45.0 | V | |
| | V ₁₂ | V _{12L} , V _{12R} | -0.3 to V ₀ + 0.3 | V | |
| | V ₄₃ | V _{43L} , V _{43R} | -0.3 to V ₀ + 0.3 | V | |
| Input voltage | V ₁ | DI ₇ -DI ₀ , XCK, LP, L/R, FR, MD, S/C, EIO ₁ , EIO ₂ , /DISPOFF, TEST ₁ , TEST ₂ | -0.3 to V _{DD} + 0.3 | V | |
| Storage temperature | T _{stg} | | -45 to +125 | °C | |

NOTES:

1. T_A = +25 °C
2. The maximum applicable voltage on any pin with respect to V_{ss} (0V).

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | APPLICABLE PINS | MIN. | TYP. | MAX. | UNIT | NOTE |
|-----------------------|------------------|-----------------------------------|-------|------|-------|------|------|
| Supply voltage(1) | V _{DD} | V _{DD} | +2.5 | | +5.5 | V | 1,2 |
| Supply voltage(2) | V ₀ | V _{0L} , V _{0R} | +10.0 | | +45.0 | V | |
| Operating temperature | T _{OPR} | | -20 | | +85 | °C | |

NOTES:

1. The applicable voltage on any pin with respect to V_{ss} (0V).
2. Ensure that voltage are set such that V_{ss} < V₄₃ < V₁₂ < V₀.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Segment Mode) ($V_{SS} = 0V$, $V_{DD} = +2.5$ to $+5.5V$, $V_0 = +10.0$ to $+45.0V$, $T_{OPR} = -20$ to $+85$ °C)

| PARAMETER | SYMBOL | CONDITIONS | APPLICABLE PINS | MIN. | TYP. | MAX. | UNIT | NOTE |
|--------------------------------------|-----------|----------------------------|--|--------------|------|-------------|-------|------|
| Input "Low" voltage | V_{IL} | | DI7-DI0, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, /DISPOFF | | | $0.2V_{DD}$ | V | |
| Input "High" voltage | V_{IH} | | | $0.8V_{DD}$ | | | V | |
| Output "Low" voltage | V_{OL} | $I_{OL} = +0.4mA$ | EIO1, EIO2 | | | +0.4 | V | |
| Output "High" voltage | V_{OH} | $I_{OH} = -0.4mA$ | | $V_{DD}-0.4$ | | | V | |
| Input leakage current | I_{LIL} | $V_I = V_{SS}$ | DI7-DI0, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, /DISPOFF | | | -10.0 | uA | |
| | I_{LIH} | $V_I = V_{DD}$ | | | | | +10.0 | uA |
| Output resistance | R_{ON} | $ \cdot V_{out} = 0.5V$ | Y1 - Y160 | | | 0.7 | 1.0 | kOhm |
| | | | | | | 1.0 | 1.5 | |
| | | | | | | 1.5 | 2.0 | |
| Standby current | I_{STB} | | V_{SS} | | | 30.0 | uA | 1 |
| Supply current(1) (Non-selection) | I_{DD1} | | V_{DD} | | | 4.0 | mA | 2 |
| Supply current(2) (Selection) | I_{DD2} | | V_{DD} | | | 4.0 | mA | 3 |
| Supply current(3) | I_o | | V_{OL}, V_{OR} | | | 500.0 | uA | 4 |

NOTES:

- $V_{DD} = +5.0V$, $V_0 = +45.0V$, $V_I = V_{SS}$.
- $V_{DD} = +5.0V$, $V_0 = +45.0V$, $f_{XCK} = 14$ MHz, non-load, $E_I = V_{DD}$. The input data is turned over by data taking clock (4-bit parallel input mode).
- $V_{DD} = +5.0V$, $V_0 = +45.0V$, $f_{XCK} = 14$ MHz, non-load, $E_I = V_{SS}$. The input data is turned over by data taking clock (4-bit parallel input mode).
- $V_{DD} = +5.0V$, $V_0 = +45.0V$, $f_{XCK} = 14$ MHz, $f_{LP} = 41.6$ kHz, $f_{FR} = 80$ Hz, non-load. The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode) ($V_{SS} = 0V$, $V_{DD} = +2.5$ to $+5.5V$, $V_0 = +10.0$ to $+45.0V$, $T_{OPR} = -20$ to $+85$ °C)

| PARAMETER | SYMBOL | CONDITIONS | APPLICABLE PINS | MIN. | TYP. | MAX. | UNIT | NOTE | |
|-------------------------|-----------|---|--|-----------------|------|-------------|---------|------|--|
| Input "Low" voltage | V_{IL} | | DI7-DI0, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, /DISPOFF | | | $0.2V_{DD}$ | V | | |
| Input "High" voltage | V_{IH} | | | $0.8V_{DD}$ | | | V | | |
| Output "Low" voltage | V_{OL} | $I_{OL} = +0.4mA$ | EIO1, EIO2 | | | +0.4 | V | | |
| Output "High" voltage | V_{OH} | $I_{OH} = -0.4mA$ | | $V_{DD}-0.4$ | | | | V | |
| Input leakage current | I_{LIL} | $V_1 = V_{SS}$ | DI7-DI0, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, /DISPOFF | | | -10.0 | μA | | |
| | I_{LIH} | $V_1 = V_{DD}$ | DI6-DI0, LP, L/R, FR, MD, S/C, /DISPOFF | | | +10.0 | μA | | |
| Input pull-down current | I_{PD} | $V_1 = V_{DD}$ | DI7, XCK, EIO1, EIO2 | | | 100.0 | μA | | |
| Output resistance | R_{ON} | $\left \frac{\partial V_{out}}{\partial I} \right = 0.5V$ | $V_0 = 40V$ | $Y_1 - Y_{160}$ | | 0.7 | 1.0 | k• | |
| | | | $V_0 = 30V$ | | | 1.0 | 1.5 | | |
| | | | $V_0 = 20V$ | | | 1.5 | 2.0 | | |
| Standby current | I_{STB} | | V_{SS} | | | 30.0 | μA | 1 | |
| Supply current(1) | I_{DD} | | V_{DD} | | | 80 | μA | 2 | |
| Supply current(2) | I_o | | V_{OL}, V_{OR} | | | 160 | μA | 2 | |

NOTES:

1. $V_{DD} = +5.0V$, $V_0 = +45.0V$, $V_1 = V_{SS}$.

2. $V_{DD} = +5.0V$, $V_0 = +45.0V$, $f_{LP} = 41.6$ kHz, $f_{FR} = 80$ Hz, 1/480 duty operation, no-load.

AC Characteristics

(Segment Mode 1) ($V_{SS} = 0V$, $V_{DD} = +4.5$ to $+5.5V$, $V_0 = +10.0$ to $+45.0V$, $T_{OPR} = -20$ to $+85$ °C)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|-----------|------------------------|------|------|------|------|------|
| Shift clock period | twck | $t_{R,tF} \cdot 10$ ns | 71 | | | ns | 1 |
| Shift clock "H" pulse width | twckh | | 23 | | | ns | |
| Shift clock "L" pulse width | twckl | | 23 | | | ns | |
| Data setup time | tDS | | 10 | | | ns | |
| Data hold time | tDH | | 20 | | | ns | |
| Latch pulse "H" pulse width | twLPH | | 23 | | | ns | |
| Shift clock rise to latch pulse rise time | tLD | | 0 | | | ns | |
| Shift clock fall to latch pulse fall time | tSL | | 25 | | | ns | |
| Latch pulse rise to shift clock rise time | tLS | | 25 | | | ns | |
| Latch pulse fall to shift clock fall time | tLH | | 25 | | | ns | |
| Enable setup time | ts | | 21 | | | ns | |
| Input signal rise time | tR | | | | 50 | ns | 2 |
| Input signal fall time | tF | | | | 50 | ns | 2 |
| /DISPOFF removal time | tSD | | 100 | | | ns | |
| /DISPOFF "L" pulse width | twDL | | 1.2 | | | us | |
| Output delay time (1) | tD | $C_L = 15$ pF | | | 40 | ns | |
| Output delay time (2) | tPD1,tPD2 | $C_L = 15$ pF | | | 1.2 | us | |
| Output delay time (3) | tPD3 | $C_L = 15$ pF | | | 1.2 | us | |

NOTES :

1. Takes the cascade connection into consideration
2. $(twck - twck_H - twck_L)/2$ is maximum in the case of high speed operation.

AC Characteristics

(Segment Mode 2) ($V_{SS} = 0V$, $V_{DD} = +2.5$ to $+4.5V$, $V_0 = +10.0$ to $+45.0V$, $T_{OPR} = -20$ to $+85$ °C)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|-----------|------------------------|------|------|------|------|------|
| Shift clock period | twck | $t_{R,Tf} \cdot 11$ ns | 125 | | | ns | 1 |
| Shift clock "H" pulse width | twckh | | 51 | | | ns | |
| Shift clock "L" pulse width | twckl | | 51 | | | ns | |
| Data setup time | tDS | | 30 | | | ns | |
| Data hold time | tDH | | 40 | | | ns | |
| Latch pulse "H" pulse width | twLPH | | 51 | | | ns | |
| Shift clock rise to latch pulse rise time | tLD | | 0 | | | ns | |
| Shift clock fall to latch pulse fall time | tSL | | 51 | | | ns | |
| Latch pulse rise to shift clock rise time | tLS | | 51 | | | ns | |
| Latch pulse fall to shift clock fall time | tLH | | 51 | | | ns | |
| Enable setup time | ts | | 36 | | | ns | |
| Input signal rise time | tR | | | | 50 | ns | 2 |
| Input signal fall time | tF | | | | 50 | ns | 2 |
| /DISPOFF removal time | tSD | | 100 | | | ns | |
| /DISPOFF "L" pulse width | twDL | | 1.2 | | | us | |
| Output delay time (1) | tD | $C_L = 15$ pF | | | 78 | ns | |
| Output delay time (2) | tPD1,tPD2 | $C_L = 15$ pF | | | 1.2 | us | |
| Output delay time (3) | tPD3 | $C_L = 15$ pF | | | 1.2 | us | |

NOTES:

1. Takes the cascade connection into consideration.
2. $(twck - twck_H - twck_L)/2$ is maximum in the case of high speed operation.

Timing Chart of Segment Mode

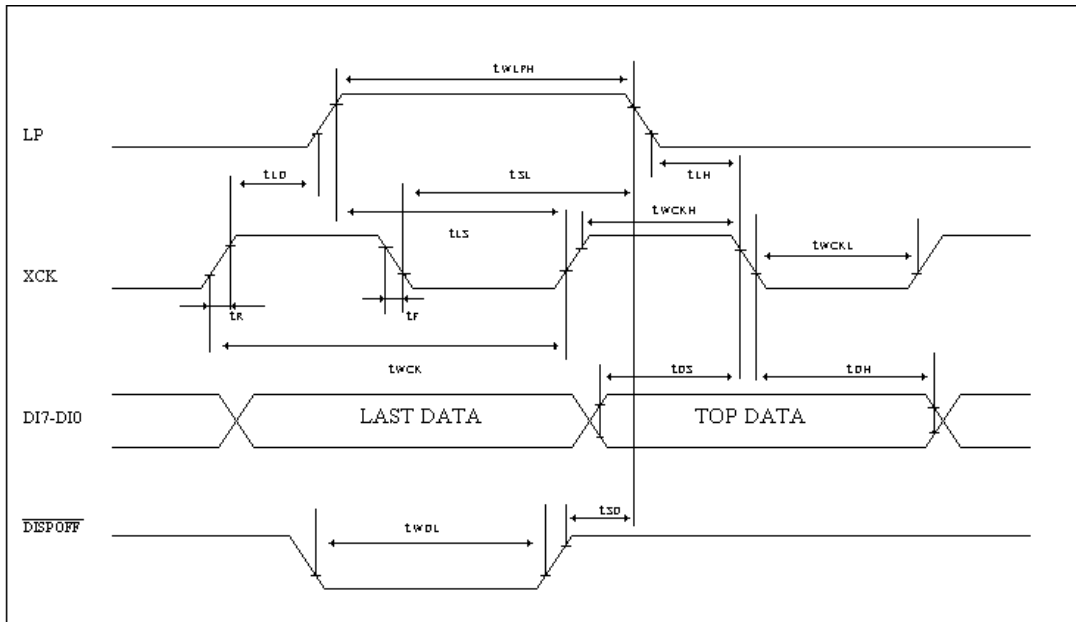


Fig. 6 Timing Characteristics (1)

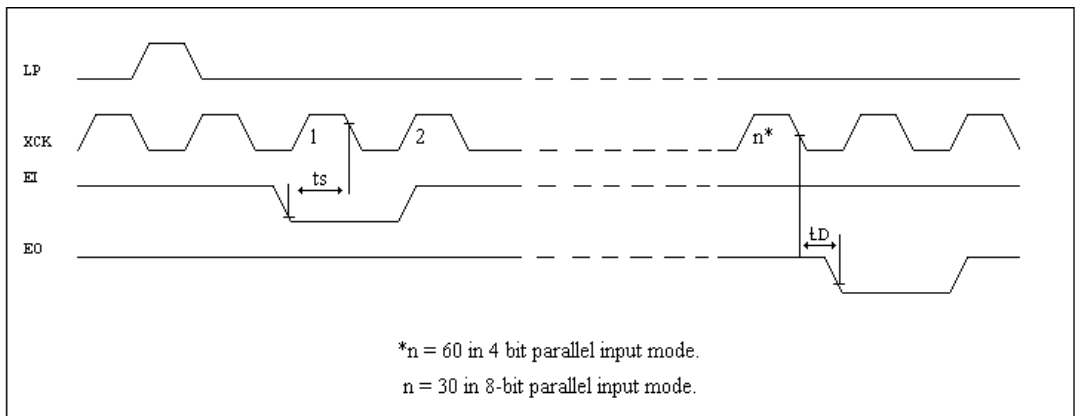


Fig. 7 Timing Characteristics (2)

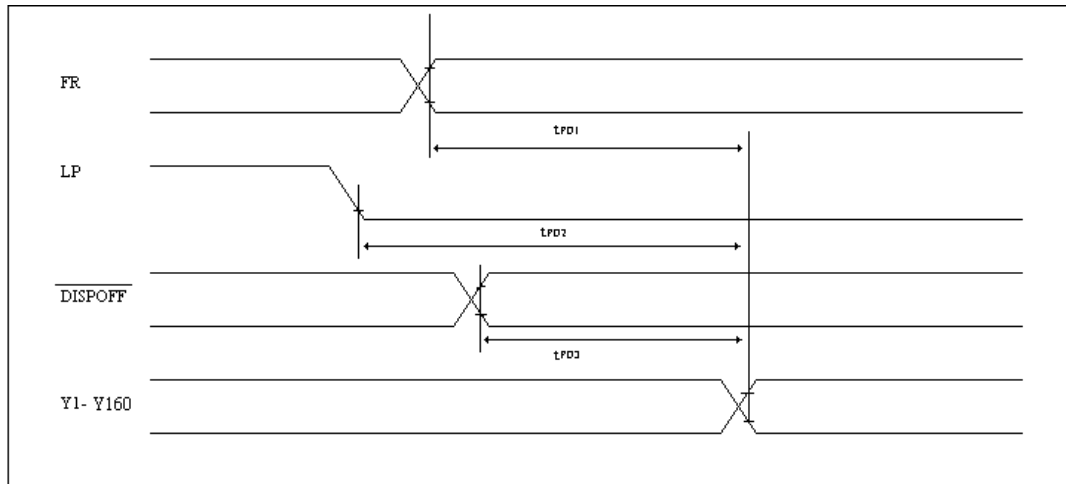
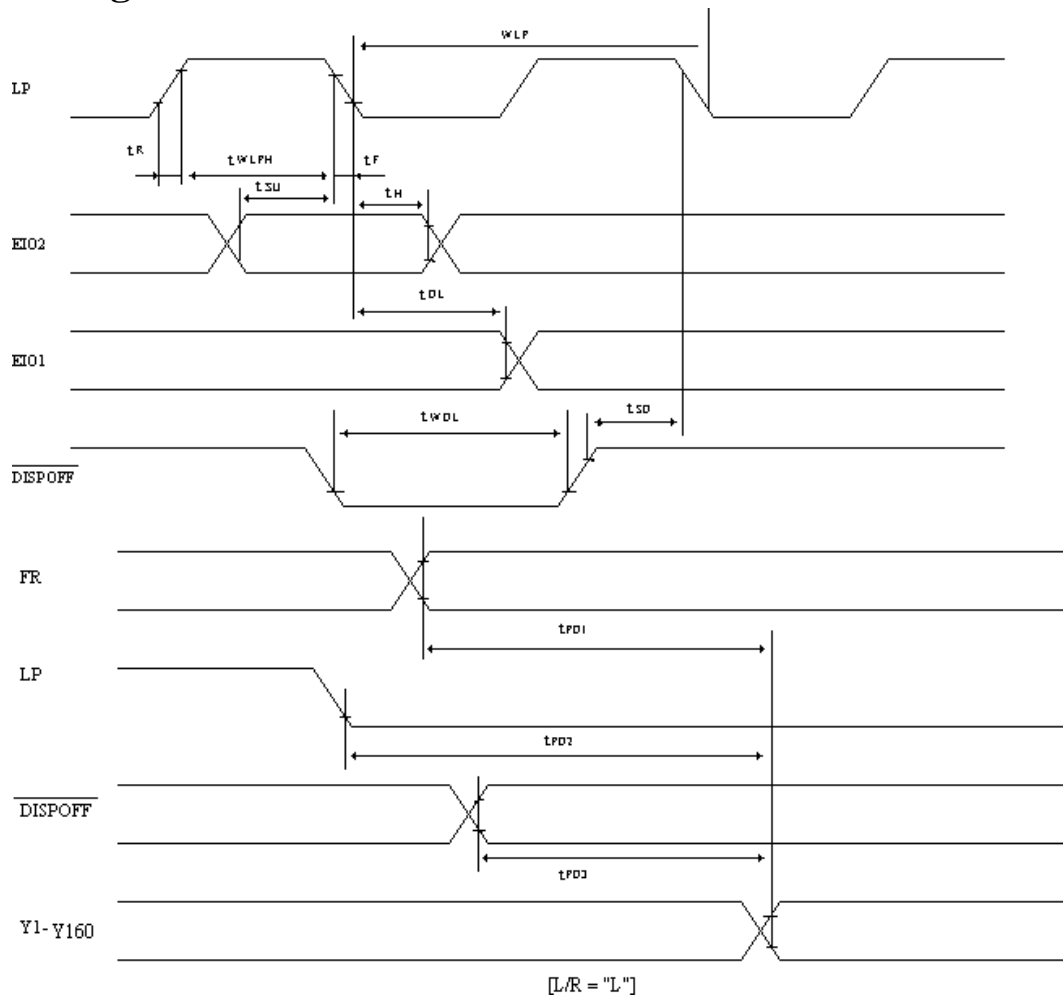


Fig. 8 Timing Characteristics (3)

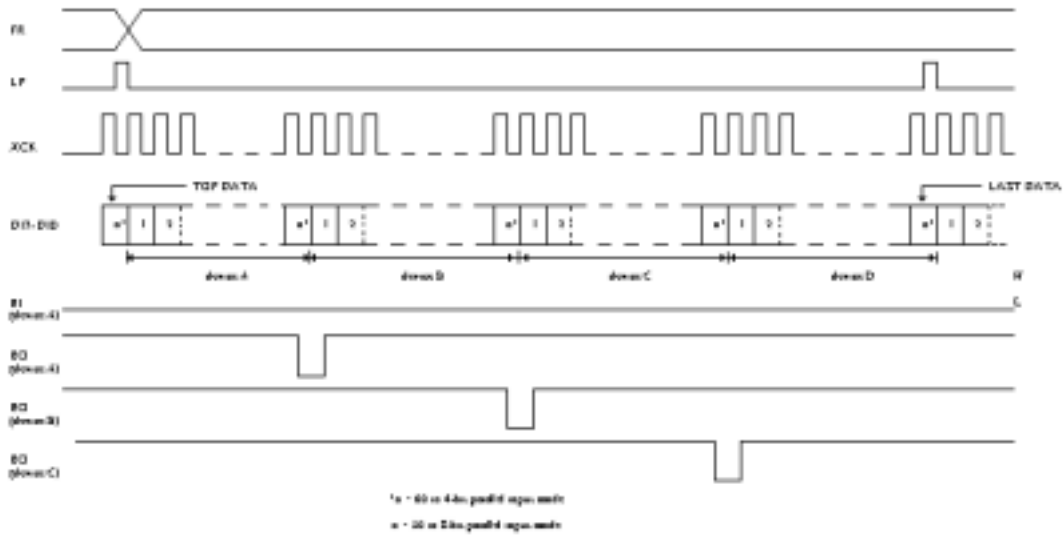
(Common Mode) ($V_{SS} = 0V$, $V_{DD} = +2.5$ to $+5.5V$, $V_0 = +10.0$ to $+45.0V$, $T_{OPR} = -20$ to $+85\text{ }^{\circ}C$)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------------------|------------|-------------------------------|------|------|------|------|
| Shift clock period | twck | $t_r, t_f \cdot 20\text{ ns}$ | 250 | | | ns |
| Shift clock "H" pulse width | twckH | $V_{DD} = +5.0 \pm 0.5V$ | 15 | | | ns |
| | | $V_{DD} = +2.5$ to $+4.5V$ | 30 | | | ns |
| Data setup time | tsu | | 30 | | | ns |
| Data hold time | th | | 50 | | | ns |
| Input signal rise time | tr | | | | 50 | ns |
| Input signal fall time | tf | | | | 50 | ns |
| /DISPOFF removal time | tSD | | 100 | | | ns |
| /DISPOFF "L" pulse width | twDL | | 1.2 | | | us |
| Output delay time (1) | tDL | $C_L = 15\text{ pF}$ | | | 200 | ns |
| Output delay time (2) | tPD1, tPD2 | $C_L = 15\text{ pF}$ | | | 1.2 | us |
| Output delay time (3) | tPD3 | $C_L = 15\text{ pF}$ | | | 1.2 | us |

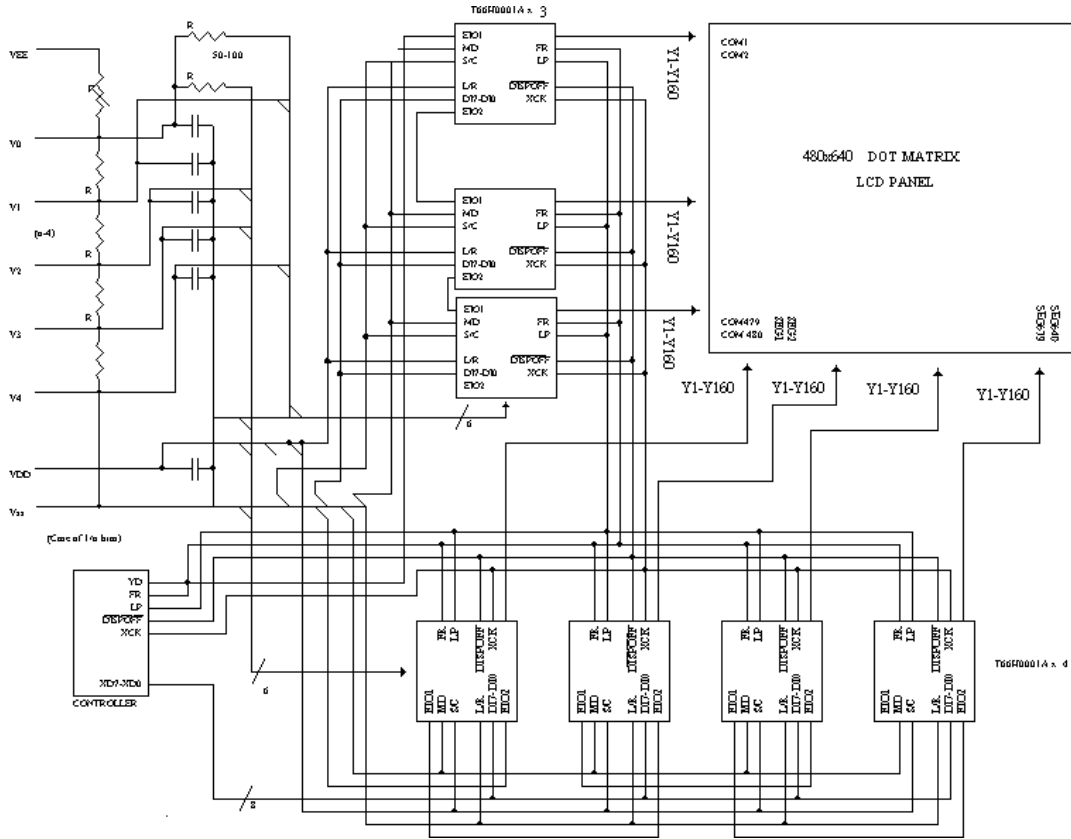
Timing Chart of Common Mode



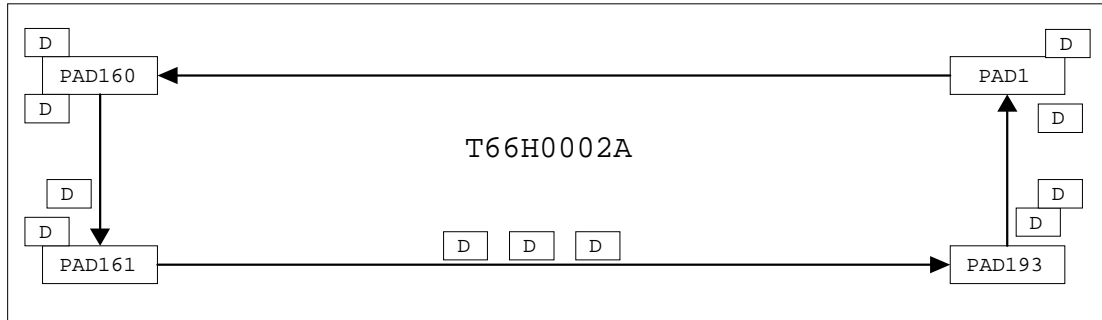
Timing Chart Of 4-Device Cascade Connection Of Segment Drivers



SYSTEM CONFIGURATION EXAMPLE



Pads List



“D” means dummy pads which are floating inside the chip.

PAD SIZE : OUTPAD = 55x72(Pad 1 to Pad 160)

INPAD = 70x72(Pad 161 to Pad 193) DUMMY = 70x80

OPEN WINDOW : OUTPAD = 29x46 INPAD = 44x46 DUMMY = 44x54

BUMP SIZE : OUTPAD = 43x60 INPAD = 54x56 DUMMY = 54x64

BUMP HEIGHT = 18

CHIP SIZE = 10100 X 1030 (WITHOUT SCRIBE LINE)

SCRIBE LINE = 80

UNIT = um

| Pad No. | Pin Name | X | Y |
|---------|----------|---------|-------|
| 1 | Y1 | 4785.95 | 398.4 |
| 2 | Y2 | 4725.95 | 398.4 |

| Pad No. | Pin Name | X | Y |
|---------|----------|---------|-------|
| 38 | Y38 | 2565.95 | 398.4 |
| 39 | Y39 | 2505.95 | 398.4 |

| | | | |
|----|-----|---------|-------|
| 3 | Y3 | 4665.95 | 398.4 |
| 4 | Y4 | 4605.95 | 398.4 |
| 5 | Y5 | 4545.95 | 398.4 |
| 6 | Y6 | 4485.95 | 398.4 |
| 7 | Y7 | 4425.95 | 398.4 |
| 8 | Y8 | 4365.95 | 398.4 |
| 9 | Y9 | 4305.95 | 398.4 |
| 10 | Y10 | 4245.95 | 398.4 |
| 11 | Y11 | 4185.95 | 398.4 |
| 12 | Y12 | 4125.95 | 398.4 |
| 13 | Y13 | 4065.95 | 398.4 |
| 14 | Y14 | 4005.95 | 398.4 |
| 15 | Y15 | 3945.95 | 398.4 |
| 16 | Y16 | 3885.95 | 398.4 |
| 17 | Y17 | 3825.95 | 398.4 |
| 18 | Y18 | 3765.95 | 398.4 |
| 19 | Y19 | 3705.95 | 398.4 |
| 20 | Y20 | 3645.95 | 398.4 |
| 21 | Y21 | 3585.95 | 398.4 |
| 22 | Y22 | 3525.95 | 398.4 |
| 23 | Y23 | 3465.95 | 398.4 |
| 24 | Y24 | 3405.95 | 398.4 |
| 25 | Y25 | 3345.95 | 398.4 |
| 26 | Y26 | 3285.95 | 398.4 |
| 27 | Y27 | 3225.95 | 398.4 |
| 28 | Y28 | 3165.95 | 398.4 |
| 29 | Y29 | 3105.95 | 398.4 |
| 30 | Y30 | 3045.95 | 398.4 |
| 31 | Y31 | 2985.95 | 398.4 |
| 32 | Y32 | 2925.95 | 398.4 |
| 33 | Y33 | 2865.95 | 398.4 |
| 34 | Y34 | 2805.95 | 398.4 |
| 35 | Y35 | 2745.95 | 398.4 |
| 36 | Y36 | 2685.95 | 398.4 |
| 37 | Y37 | 2625.95 | 398.4 |

| | | | |
|----|-----|---------|-------|
| 40 | Y40 | 2445.95 | 398.4 |
| 41 | Y41 | 2385.95 | 398.4 |
| 42 | Y42 | 2325.95 | 398.4 |
| 43 | Y43 | 2265.95 | 398.4 |
| 44 | Y44 | 2205.95 | 398.4 |
| 45 | Y45 | 2145.95 | 398.4 |
| 46 | Y46 | 2085.95 | 398.4 |
| 47 | Y47 | 2025.95 | 398.4 |
| 48 | Y48 | 1965.95 | 398.4 |
| 49 | Y49 | 1905.95 | 398.4 |
| 50 | Y50 | 1845.95 | 398.4 |
| 51 | Y51 | 1785.95 | 398.4 |
| 52 | Y52 | 1725.95 | 398.4 |
| 53 | Y53 | 1665.95 | 398.4 |
| 54 | Y54 | 1605.95 | 398.4 |
| 55 | Y55 | 1545.95 | 398.4 |
| 56 | Y56 | 1485.95 | 398.4 |
| 57 | Y57 | 1425.95 | 398.4 |
| 58 | Y58 | 1365.95 | 398.4 |
| 59 | Y59 | 1305.95 | 398.4 |
| 60 | Y60 | 1245.95 | 398.4 |
| 61 | Y61 | 1185.95 | 398.4 |
| 62 | Y62 | 1125.95 | 398.4 |
| 63 | Y63 | 1065.95 | 398.4 |
| 64 | Y64 | 1005.95 | 398.4 |
| 65 | Y65 | 945.95 | 398.4 |
| 66 | Y66 | 885.95 | 398.4 |
| 67 | Y67 | 825.95 | 398.4 |
| 68 | Y68 | 765.95 | 398.4 |
| 69 | Y69 | 705.95 | 398.4 |
| 70 | Y70 | 645.95 | 398.4 |
| 71 | Y71 | 585.95 | 398.4 |
| 72 | Y72 | 525.95 | 398.4 |
| 73 | Y73 | 465.95 | 398.4 |
| 74 | Y74 | 405.95 | 398.4 |

| Pad No. | Pin Name | X | Y |
|---------|----------|--------|-------|
| 75 | Y75 | 345.95 | 398.4 |

| Pad No. | Pin Name | X | Y |
|---------|----------|----------|-------|
| 112 | Y112 | -1906.25 | 398.4 |

| | | | |
|-----|------|----------|-------|
| 76 | Y76 | 285.95 | 398.4 |
| 77 | Y77 | 225.95 | 398.4 |
| 78 | Y78 | 165.95 | 398.4 |
| 79 | Y79 | 105.95 | 398.4 |
| 80 | Y80 | 46.95 | 398.4 |
| 81 | Y81 | -46.25 | 398.4 |
| 82 | Y82 | -106.25 | 398.4 |
| 83 | Y83 | -166.25 | 398.4 |
| 84 | Y84 | -226.25 | 398.4 |
| 85 | Y85 | -286.25 | 398.4 |
| 86 | Y86 | -346.25 | 398.4 |
| 87 | Y87 | -406.25 | 398.4 |
| 88 | Y88 | -466.25 | 398.4 |
| 89 | Y89 | -526.25 | 398.4 |
| 90 | Y90 | -586.25 | 398.4 |
| 91 | Y91 | -646.25 | 398.4 |
| 92 | Y92 | -706.25 | 398.4 |
| 93 | Y93 | -766.25 | 398.4 |
| 94 | Y94 | -826.25 | 398.4 |
| 95 | Y95 | -886.25 | 398.4 |
| 96 | Y96 | -946.25 | 398.4 |
| 97 | Y97 | -1006.25 | 398.4 |
| 98 | Y98 | -1066.25 | 398.4 |
| 99 | Y99 | -1126.25 | 398.4 |
| 100 | Y100 | -1186.25 | 398.4 |
| 101 | Y101 | -1246.25 | 398.4 |

| | | | |
|-----|------|----------|-------|
| 113 | Y113 | -1966.25 | 398.4 |
| 114 | Y114 | -2026.25 | 398.4 |
| 115 | Y115 | -2086.25 | 398.4 |
| 116 | Y116 | -2146.25 | 398.4 |
| 117 | Y117 | -2206.25 | 398.4 |
| 118 | Y118 | -2266.25 | 398.4 |
| 119 | Y119 | -2326.25 | 398.4 |
| 120 | Y120 | -2386.25 | 398.4 |
| 121 | Y121 | -2446.25 | 398.4 |
| 122 | Y122 | -2506.25 | 398.4 |
| 123 | Y123 | -2566.25 | 398.4 |
| 124 | Y124 | -2626.25 | 398.4 |
| 125 | Y125 | -2686.25 | 398.4 |
| 126 | Y126 | -2746.25 | 398.4 |
| 127 | Y127 | -2806.25 | 398.4 |
| 128 | Y128 | -2866.25 | 398.4 |
| 129 | Y129 | -2926.25 | 398.4 |
| 130 | Y130 | -2986.25 | 398.4 |
| 131 | Y131 | -3046.25 | 398.4 |
| 132 | Y132 | -3106.25 | 398.4 |
| 133 | Y133 | -3166.25 | 398.4 |
| 134 | Y134 | -3226.25 | 398.4 |
| 135 | Y135 | -3286.25 | 398.4 |
| 136 | Y136 | -3346.25 | 398.4 |
| 137 | Y137 | -3406.25 | 398.4 |
| 138 | Y138 | -3466.25 | 398.4 |

| | | | |
|-----|------|--------------|-------|
| 102 | Y102 | -1306.2 5 | 398.4 |
| 103 | Y103 | -1366.2 5 | 398.4 |
| 104 | Y104 | -1426.2 5 | 398.4 |
| 105 | Y105 | -1486.2 5 | 398.4 |
| 106 | Y106 | -1546.2 5 | 398.4 |
| 107 | Y107 | -1606.2 5 | 398.4 |
| 108 | Y108 | -1666.2 5 | 398.4 |
| 109 | Y109 | -1726.2 5 | 398.4 |
| 110 | Y110 | -1786.2 5 | 398.4 |
| 111 | Y111 | -1846.2 5 | 398.4 |

| | | | |
|-----|------|--------------|-------|
| 139 | Y139 | -3526.2 5 | 398.4 |
| 140 | Y140 | -3586.2 5 | 398.4 |
| 141 | Y141 | -3646.2 5 | 398.4 |
| 142 | Y142 | -3706.2 5 | 398.4 |
| 143 | Y143 | -3766.2 5 | 398.4 |
| 144 | Y144 | -3826.2 5 | 398.4 |
| 145 | Y145 | -3886.2 5 | 398.4 |
| 146 | Y146 | -3946.2 5 | 398.4 |
| 147 | Y147 | -4006.2 5 | 398.4 |
| 148 | Y148 | -4066.2 5 | 398.4 |

| Pad No. | Pin Name | X | Y |
|---------|----------|--------------|-------|
| 149 | Y149 | -4126.2 5 | 398.4 |
| 150 | Y150 | -4186.2 5 | 398.4 |
| 151 | Y151 | -4246.2 5 | 398.4 |
| 152 | Y152 | -4306.2 5 | 398.4 |
| 153 | Y153 | -4366.2 5 | 398.4 |
| 154 | Y154 | -4426.2 5 | 398.4 |
| 155 | Y155 | -4486.2 5 | 398.4 |
| 156 | Y156 | -4546.2 5 | 398.4 |
| 157 | Y157 | -4606.2 5 | 398.4 |
| 158 | Y158 | -4666.2 5 | 398.4 |
| 159 | Y159 | -4726.2 5 | 398.4 |
| 160 | Y160 | -4786.2 5 | 398.4 |
| 161 | V0L | -4754.4 | -434 |
| 162 | V0L | -4669.4 | -434 |
| 163 | V12L | -4541.0 5 | -434 |

| Pad No. | Pin Name | X | Y |
|---------|----------|---------|--------|
| 182 | DISPOFF | 2897.6 | -434 |
| 183 | LP | 3169.4 | -434 |
| 184 | EIO1 | 3259.4 | -434 |
| 185 | FR | 3531.2 | -434 |
| 186 | MD | 3621.2 | -434 |
| 187 | GND | 3809.8 | -434 |
| 188 | GND | 3894.8 | -434 |
| 189 | V5R | 4270.8 | -434 |
| 190 | V43R | 4398.5 | -434 |
| 191 | V12R | 4541.05 | -434 |
| 192 | V0R | 4669.4 | -434 |
| 193 | V0R | 4754.4 | -434 |
| | | | |
| Dummy | RT | 4970 | 319.75 |
| | | 4891.35 | 429.85 |

| | | | |
|-----|------|---------|------|
| 164 | V43L | -4398.5 | -434 |
| 165 | V5L | -4270.8 | -434 |
| 166 | GND | -3894.8 | -434 |
| 167 | GND | -3809.8 | -434 |
| 168 | LR16 | -3621.2 | -434 |
| 169 | VDD | -3531.2 | -434 |
| 170 | VDD | -3446.2 | -434 |
| 171 | SC | -3356.2 | -434 |
| 172 | EIO2 | -3084.4 | -434 |
| 173 | DI0 | -2994.4 | -434 |
| 174 | DI1 | -2722.6 | -434 |
| 175 | DI2 | -2632.6 | -434 |
| 176 | DI3 | -2360.8 | -434 |
| 177 | DI4 | 2084 | -434 |
| 178 | DI5 | 2174 | -434 |
| 179 | DI6 | 2445.8 | -434 |
| 180 | DI7 | 2535.8 | -434 |
| 181 | XCK | 2807.6 | -434 |

| | | | |
|--|--------|--------------|---------|
| | LT | -4891.3 5 | 429.85 |
| | | -4970 | 319.75 |
| | LB | -4970 | -340.4 |
| | | -4874.5 | -429.85 |
| | RB | 4874.5 | -429.85 |
| | | 4970 | -340.4 |
| | Middle | -1954.6 5 | -429.85 |
| | | -1713.7 5 | -435 |
| | | 1842.3 | -429.85 |

Appendix

